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Reg. No. : .....

Name : .....

Eighth Semester B.Tech. Degree Examination, November 2013
(2008 Scheme)
08.802 : COMPUTER SYSTEM ARCHITECTURE (R)

Time : 3 Hours Max. Marks : 100

PART – A

(Answer **all** questions.)

1. Define the following terms for various system interconnect architectures :
   a) Node degree
   b) Network diameter
   c) Bisection bandwidth
   d) Network latency.

2. Distinguish between implicit parallelism and explicit parallelism of parallel programming.

3. Describe different types of hazards due to data dependency.

4. What is the significance of Bernstein's condition to detect parallelism ?

5. Write a short note on CPA and CSA.

6. Define a base scalar processor and illustrate the execution of successive instruction in a base scalar processor by a space-time diagram.

7. Distinguish between register-to-register and memory-to memory architecture for building conventional multivector super computers.

8. Give an overview about the memory level hierarchy.

9. Differentiate between write-through laches and write-back laches.

10. Write a short note on interleaved memory organization in multiprocessor system.

(10×4=40 Marks)

PART – B

Module – I

11. Distinguish between multiprocessors and multi computers based on their structures, resource sharing and interprocessor communications. Also explain the differences among UMA, NUMA, COMA and NORMA computers. **20**

OR

12. a) Describe briefly about the operational model of SIMD computers with an examples. **10**

b) Answer the following questions for the K-ary n-cube network.

I) What is the network diameter, bisection bandwidth ?

II) What is the node degree and number of nodes ?

III) Under the assumption of constant wire bisection, why do low-dimensional networks (tort) have lower latency and higher hot-spot through put than high-dimensional networks (hypercubes) ?

IV) Mention the difference between a conventional torus and a folded torus. **10**

Module – II

13. Explain the concept of pipelining in

i) Superscalar processors

ii) VLIW processors. **20**

OR

14. Consider the following pipeline reservation table

	1	2	3	4
S1	X			X
S2		X		
S3			X	

1) What are the forbidden latencies ?

2) Draw the state transition diagram.

3) List all the simple cycles and greedy cycles.

4) Determine the optional constant latency cycle and the minimal average latency.

5) Let the pipeline clock period be $\lambda = 20$ ns. Determine the throughput of this pipeline. **20**

Module – III

15. a) Describe how crossbar switch and multiport memories are used in multistage networks. **15**

b) Distinguish between static and dynamic dataflow computers. **5**

OR

16. Explain the following Cache Coherence Protocol.

a) Snoopy Bus Protocol

b) Full map directory based protocol. **20**